In the Claims:

Please amend the claims as indicated hereafter.

1. (Currently Amended) A computer system for processing instructions of computer programs, comprising:

a register;

a pipeline configured to execute instructions of a computer program, said pipeline having a first stage and a second stage; [[and]]

first circuitry configured to read a first predicate value from said register and to receive a second predicate value, said first circuitry configured to ~~transmit, to said first stage, said first predicate value and to~~ select between at least said second predicate value and said first predicate value read from said register, said first circuitry further configured to transmit, ~~transmit said selected predicate~~ to said first stage, the value ~~to said second stage~~ selected by said first circuitry; and

second circuitry configured to select between at least a third predicate value and said value selected by said first circuitry, said second circuitry further configured to transmit, to said second stage, the value selected by said second circuitry.

2. (Previously Presented) The system of claim 1, wherein said predicate value selected by said circuitry is said first predicate value read from said register.

3. (Previously Presented) The system of claim 1, wherein said predicate value selected by said circuitry is said second predicate value.

4. (Currently Amended) ~~The system of claim 1,~~ A computer system for processing instructions of computer programs, comprising:

a register;

a pipeline configured to execute instructions of a computer program, said pipeline having a first stage and a second stage; and

circuitry configured to read a first predicate value from said register and to receive a second predicate value, said circuitry configured to transmit, to said first stage, said first predicate value and to select between at least said second predicate value and said first predicate value read from said register, said circuitry further configured to transmit said selected predicate value to said second stage, ~~wherein~~ said circuitry [[is]] further configured to detect whether an instruction in said second stage is stalled and to select said selected predicate value based on whether said instruction in said second stage is stalled.

5. (Previously Presented) The system of claim 1, wherein said circuitry includes a latch that is configured to receive said selected predicate value and to transmit said selected predicate value to said second stage in response to an edge of a clock signal.

6. (Previously Presented) A computer system, comprising:

a register;

a pipeline configured to execute instructions of a computer program, said pipeline having a first stage and a second stage;

first circuitry coupled to said register and to said first stage, said first circuitry configured to simultaneously receive a first plurality of predicate values, at least one of said first plurality of predicate values received from said register and each of said first plurality of predicate values associated with one of said instructions, said first circuitry configured to select a predicate value among said first plurality of simultaneously received predicate values, said first circuitry further configured to transmit said predicate value selected among said first plurality of predicate values to said first stage and across a connection; and

second circuitry coupled to said connection and to said second stage, said second circuitry configured to simultaneously receive a second plurality of predicate values, said second plurality of predicate values including said predicate value transmitted across said connection and each of said second plurality of predicate values associated with said one instruction, said second circuitry configured to select a predicate value among said second plurality of simultaneously received predicate values and to transmit, to said second stage, said predicate value selected among said second plurality of predicate values.

7. (Previously Presented) The system of claim 6, wherein said second circuitry includes a latch configured to receive said predicate value selected among said second plurality of predicate values and to transmit said predicate value received by said latch in response to an edge of a clock signal.

8. (Original) The system of claim 6, wherein one of said second plurality of predicate values is transmitted from another pipeline.

9-10. (Canceled).

11. (Previously Presented) The system of claim 6, further comprising control circuitry configured to compare register identifiers defined by said instructions and to transmit control signals to said first and second circuitry, wherein said first circuitry is configured to select said predicate value selected among said first plurality of predicate values based on at least one of said control signals and said second circuitry is configured to select said predicate value selected among said second plurality of predicate values based on at least one of said control signals.

12. (Previously Presented) A method for processing instructions of computer programs, comprising the steps of:

providing a pipeline having a first stage and a second stage;

producing a predicate value;

writing said predicate value to a register;

receiving an instruction;

receiving a control signal;

reading said predicate value from said register based on a register identifier included in said instruction;

transmitting said predicate value read from said register in said reading step to said first stage of said pipeline;

processing said instruction via said first stage of said pipeline based on said predicate value transmitted to said first stage;

receiving a new predicate value;

selecting, based on said control signal, between said new predicate value and said predicate value read from said register in said reading step;

transmitting said predicate value selected in said selecting step to said second stage of said pipeline; and

processing said instruction via said second stage based on said predicate value selected in said selecting step.

13. (Original) The method of claim 12, wherein said one predicate value selected in said selecting step is said predicate value read in said reading step.

14. (Original) The method of claim 12, wherein said predicate value selected in said selecting step is said new predicate value, said selecting step further including the step of ignoring said predicate value read in said reading step.

15. (Original) The method of claim 12, further comprising the steps of:

detecting whether said instruction is stalled; and

performing said selecting step based on said detecting step.

16. (Original) The method of claim 12, further comprising the steps of:

detecting whether said new predicate value is indicative of a predicate status of said instruction; and

performing said selecting step based on said detecting step.

17. (Original) The method of claim 12, further comprising the steps of:

receiving a second new predicate value;

selecting between said second new predicate value and said value transmitted to said second circuitry;

detecting that said instruction is stalled; and

performing said selecting between said second new predicate value step in response to said detecting step.

18. (Previously Presented) A method for processing instructions of computer programs, comprising the steps of:

providing a pipeline having a first stage and a second stage;

reading a predicate value from a register;

simultaneously receiving a first plurality of predicate values, said first plurality of predicate values including said predicate value read from said register;

selecting a predicate value among said first plurality of simultaneously received predicate values;

transmitting, to said first stage of said pipeline, said predicate value selected in said selecting one of said first plurality of predicate values;

processing an instruction in said first stage of said pipeline based on said predicate value transmitted to said first stage;

simultaneously receiving a second plurality of predicate values, said second plurality of predicate values including said predicate value selected among said first plurality of predicate values, each of said second plurality of predicate values associated with said instruction;

selecting a predicate value among said second plurality of predicate values;

transmitting said predicate value selected among said second plurality of predicate values to said second stage of said pipeline; and

processing said instruction in said second stage of said pipeline based on said predicate value transmitted to said second stage.

19-20. (Canceled).

21. (Currently Amended) ~~The system of claim 5,~~ A computer system for processing instructions of computer programs, comprising:

a register;

a pipeline configured to execute instructions of a computer program, said pipeline having a first stage and a second stage; and

circuitry configured to read a first predicate value from said register and to receive a second predicate value, said circuitry configured to transmit, to said first stage, said first predicate value and to select between at least said second predicate value and said first predicate value read from said register, said circuitry further configured to transmit said selected predicate value to said second stage, wherein said circuitry includes a latch that is configured to receive said selected predicate value and to transmit said selected predicate value to said second stage in

response to an edge of a clock signal, and wherein second predicate value is received by said circuitry from another latch.

22. (Currently Amended) ~~The system of claim 5,~~ A computer system for processing instructions of computer programs, comprising:

a register;

a pipeline configured to execute instructions of a computer program, said pipeline having a first stage and a second stage; and

circuitry configured to read a first predicate value from said register and to receive a second predicate value, said circuitry configured to transmit, to said first stage, said first predicate value and to select between at least said second predicate value and said first predicate value read from said register, said circuitry further configured to transmit said selected predicate value to said second stage, wherein said circuitry includes a latch that is configured to receive said selected predicate value and to transmit said selected predicate value to said second stage in response to an edge of a clock signal, and wherein said second predicate value is received by said circuitry from said latch.

23. (Previously Presented) The system of claim 7, wherein said second plurality of predicate values includes an output value of said latch.

24. (Currently Amended) A system for processing instructions of computer programs, comprising:

a pipeline configured to execute an instruction of a computer program, said pipeline having a first stage and a second stage; [[and]]

first circuitry configured to read a first predicate value from a register and ~~to transmit, to said first stage, said first predicate value read from said register, said circuitry configured~~ to select one predicate value among a first plurality of predicate values, said first plurality of predicate values including said first predicate value read from said register, said first circuitry further configured to ~~transmit said selected predicate value to said second stage,~~ transmit, to said first stage, the value selected by said first circuitry; and

second circuitry configured to receive, from said first circuitry, said value selected by said first circuitry, said second circuitry configured to select one predicate value among a second plurality of predicate values, said second plurality of predicate values including said value selected by said first circuitry, said second circuitry further configured to transmit, to said second stage, the value selected by said second circuitry,

wherein said first stage is configured to process said instruction based on said first predicate value transmitted to said first stage, and wherein said second stage is configured to process said instruction based on said selected predicate value.

25. (Previously Presented) The system of claim 24, wherein said circuitry comprises a latch configured to receive said selected predicate value and to output said selected predicate value based on a clock signal, and wherein said plurality of predicate values includes an output value of said latch.